	Type	L #	Hits	Search Text	DBs
1	BRS	L1	1	(emitter near3 pad) near25 (intrinsic near3 base)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
2	BRS	L2	1	(emitter near3 land$3) near25 (intrinsic near3 base)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
3	BRS	L3	1726	(emitter) near25 (intrinsic near3 base)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
4	BRS	L4	6	3 and (land$3 near pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
5	BRS	L5	2	(emitter) near25 (intrinsic near3 base) near25 (land$3 near5 pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
6	BRS	L6	2	(emitter) near25 (intrinsic near3 base) same (land$3 near5 pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
7	BRS	L7	6	(emitter) near25 (intrinsic near3 base) and (land$3 near5 pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
8	BRS	L8	7	(intrinsic near3 base) and (land$3 near5 emitter near5 pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
9	BRS	L9	61	(intrinsic near3 base) and (emitter near5 pad)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
10	BRS	L10	2	"5541121".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
11	BRS	L11	2	"5506157".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	U	1	Document ID	Title
1			US 20050048735 A1	BIPOLAR TRANSISTOR HAVING RAISED EXTRINSIC BASE WITH SELECTABLE SELF-ALIGNMENT AND METHODS OF FORMING SAME
2			US 20040262713 A1	High fT and fmax Bipolar Transistor and Method of Making Same
3			US 20040224461 A1	Method to fabricate high-performance NPN transistors in a BiCMOS process
4			US 20040222497 A1	METHOD TO FABRICATE HIGH-PERFORMANCE NPN TRANSISTORS IN A BICMOS PROCESS
5			US 6869852 B1	Self-aligned raised extrinsic base bipolar transistor structure and method
6			US 6809024 B1	Method to fabricate high-performance NPN transistors in a BiCMOS process